FINAL REPORT

for

DESIGN OF LOW STRESS SWITCHING ELECTRONICS FOR EMA APPLICATIONS

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INTRODUCTION

The Component Development Division of the Propulsion Laboratory at Marshall Space Flight Center (MSFC) is currently developing a class of electromechanical actuators (EMAs) for use in space transportation applications such as Thrust Vector Control (TVC) and Propellant Control Valves (PCV). These high power servomechanisms will require rugged, reliable and compact power electronic modules capable of modulating several hundred amperes of current at up to 270 volts.

One of the key elements in the EMA system is the three-phase inverter which modulates the flow of energy into the brushless dc motor in the system. Efforts at MSFC have been centered around Pulse Width Modulation (PWM) technology for controller implementation. Under a previous task order, Auburn University developed a low power PDM controller for a brushless dc motor which utilized both MOS-Controlled Thyristors (MCT) and Insulated Gate Bipolar Transistors (IGBT) in the drive (current) stage [1]. This controller operated in a rate control configuration. The speed of the brushless dc motor is proportional to the applied stator voltage. In a PDM system, the control system determines the number of resonant voltage pulses which must be applied to the stator to achieve a desired speed. The addition of a waveshaping circuit to the front end of a standard three-phase inverter yields a resonant dc link (RDCL) inverter. The resonant voltage pulses which are applied to the stator are produced through the action of this waveshaping circuit and the inverter.

The RDCL inverter has two primary drawbacks. First, the amplitude of the resonant voltage pulses necessary to produce zero-voltage switching can easily exceed twice the bus voltage [2-3], depending on the circuit operating conditions. For example, on the 270 Vdc system considered for EMAs, the amplitude of the resonant pulses may exceed 540 volts. This is of particular importance for space vehicles which operate in environments where the breakdown voltage is greatly reduced compared to terrestrial levels. Another drawback with a PDM system is that the inverter switches may only be changed during the instances of time when the input voltage to the inverter is clamped at zero. Therefore, the number of potential switching instances is reduced in comparison to a pulse-width modulated (PWM) system which has in essence an infinite number of potential switching instances. The disadvantage of a reduced number of potential switching instances is somewhat offset by the higher switching frequencies possible with an RDCL inverter.

A second project investigated the application of zero-voltage switching techniques in a PWM-like system where the bus voltage is clamped at 270 V [4]. In the same manner as the RDCL inverter, the inverter selected for this implementation was a combination of a waveshaping circuit and a standard three-phase inverter. The function of the waveshaping circuit is analogous to the clutch in a mechanical transmission. When the state of an inverter switch needs to be changed, the waveshaping circuit disconnects the inverter from the power source and clamps the inverter input voltage to zero. The states of the inverter switches are changed and then the waveshaping circuit reconnects the power source. Two different inverter systems were constructed under this project: one

was tested at Auburn University and the other at Marshall Space Flight Center. These controllers had the following limitations:

1) the Hall effect signals from the brushless dc motor were decoded by an LM 621 integrated circuit manufactured by National Semiconductor. This chip was discontinued in 1994.

2) the voltage source inverter in these controllers utilizes a current loop to control the current flow into the motor. A single current sensor on the dc link provided the input to the current loop as opposed to most approaches which use either two or three sensors. The use of a single sensor made tuning the control circuitry more difficult.

3) the control circuit required substantial tuning to achieve proper circuit operation. The circuit performed satisfactorily once the control circuitry was tuned.

This project has focused on improving the controllers by addressing these limitations. The Hall signal decoding was performed using GAL technology, which permits greater flexibility. A single GAL device may be utilized with many different motors by simply reprogramming the device. In the comparison between a single current sensor versus three current sensors, it was decided to continue to use only one sensor primarily because of space limitations in the controller. A change in the waveshaping circuit employed with a standard three-phase inverter permitted a reduction in control circuit tuning. This was accomplished because the number of semiconductor switches was reduced and one capacitor was eliminated.

The next chapter of this report will present the inverter implemented for this project. The operation of the waveshaping circuit will be described through analysis and waveforms. Design relationships will also be presented. Chapter 3 contains the design

and implementation of a system for the MSFC electromechanical actuation testbed. Experimental results are presented in Chapter 4. Project conclusions are contained in Chapter 5.

Chapter 2

OPERATION AND ANALYSIS OF THE PARALLEL RESONANT DC-LINK

The EMA testbed at MSFC utilizes a brushless dc motor to control the position of a linear actuator. Presently, the approach utilized at MSFC is that the motor is driven by a three-phase current source inverter. In high power applications such as this, switching of the large inductive motor currents results in considerable switching losses/stresses in the semiconductors that make up the inverter. Another negative consequence of hard switching is EMI which is currently a significant problem. However, these problems can be eliminated by soft-switching the inverter semiconductors. Soft-switching is achieved by turning the switches on/off under either zero voltage or current conditions.

This chapter will present the waveshaping circuit which allows the zero-voltage switching (ZVS) of the inverter switches to be achieved. The operation of the parallel resonant dc link circuit can be divided into six different modes of operation. On the pages that follow, an equivalent circuit for the six modes of the link circuit will be given and described in detail. Additionally, equations pertinent to each mode will be developed in order to further describe circuit operation.

ZVS Inverter Topology

The zero-voltage switching characteristics of the inverter are achieved by the addition of a waveshaping circuit at the input to the inverter. There are many examples of waveshaping circuits that will achieve this function and several have been explored in the past [1,4]. The particular waveshaping circuit chosen, a parallel resonant dc-link (PRDCL) converter is shown in Figure 2.1, was selected due to several factors. Most importantly, the circuit utilizes only three semiconductor switches and a single resonant capacitor and inductor. These elements provide for increased reliability over other choices. Furthermore, this circuit also eliminates the problems

associated with a resonant dc link [1] inverter such as voltage peaks that could easily exceed the breakdown voltage in the space environment. The PRDCL also provides for a variable zero-voltage interval which is a different feature from other parallel resonant links. This feature allows for further enhancement of PWM capabilities as the zero voltage interval is limited only by the component losses.

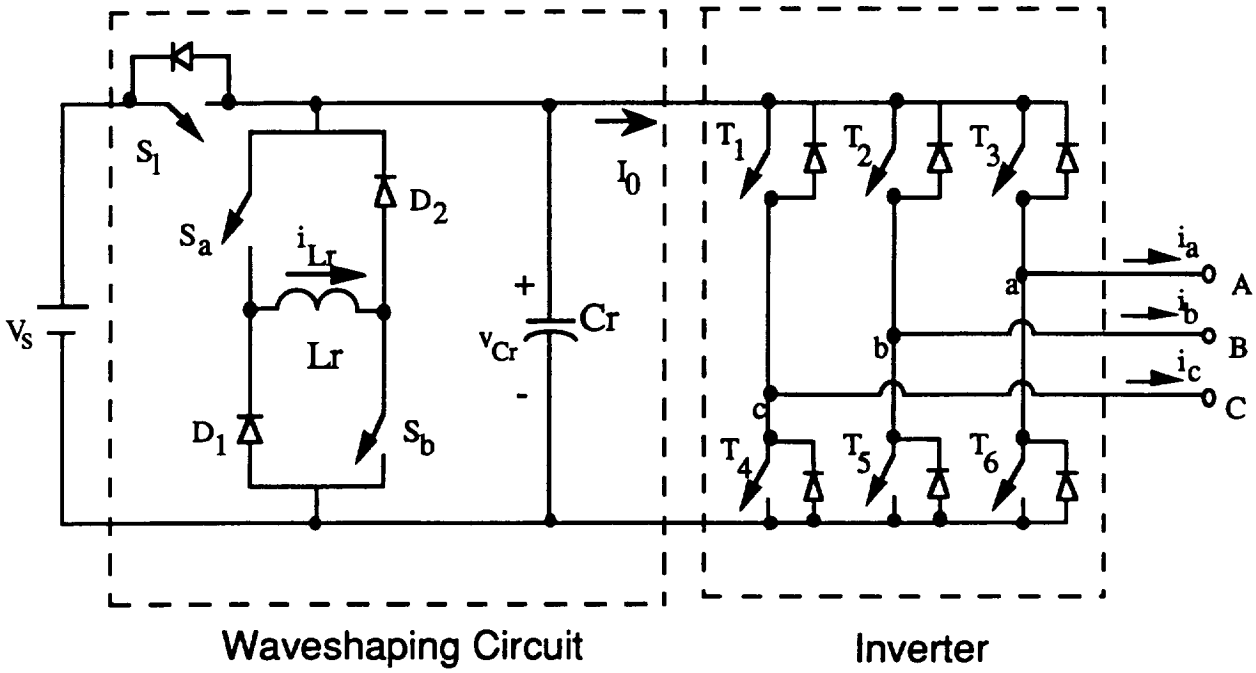

Figure 2.1. ZVS Inverter with Parallel Resonant DC-Link [5].

The different modes of the waveshaping circuit will now be discussed with the aid of Figures 2.2 and 2.3 which depicts the waveshaping circuit and the waveforms associated with it. All circuit components in Figure 2.3 are considered ideal. A shunt switch, Sr, across the resonant capacitor is added in order to reduce ringing during the zero voltage interval. Additionally, the inverter currrent is assumed to be constant during the operation of the waveshapaing circuit and is therefore replaced by a current source Io. This assumption is valid assuming the load inductance is much larger than the resonant inductor Lr. Discussion of the circuit operation will begin by assuming steady state conditions with the voltage source Vs supplying energy to the inverter through switch Sl.

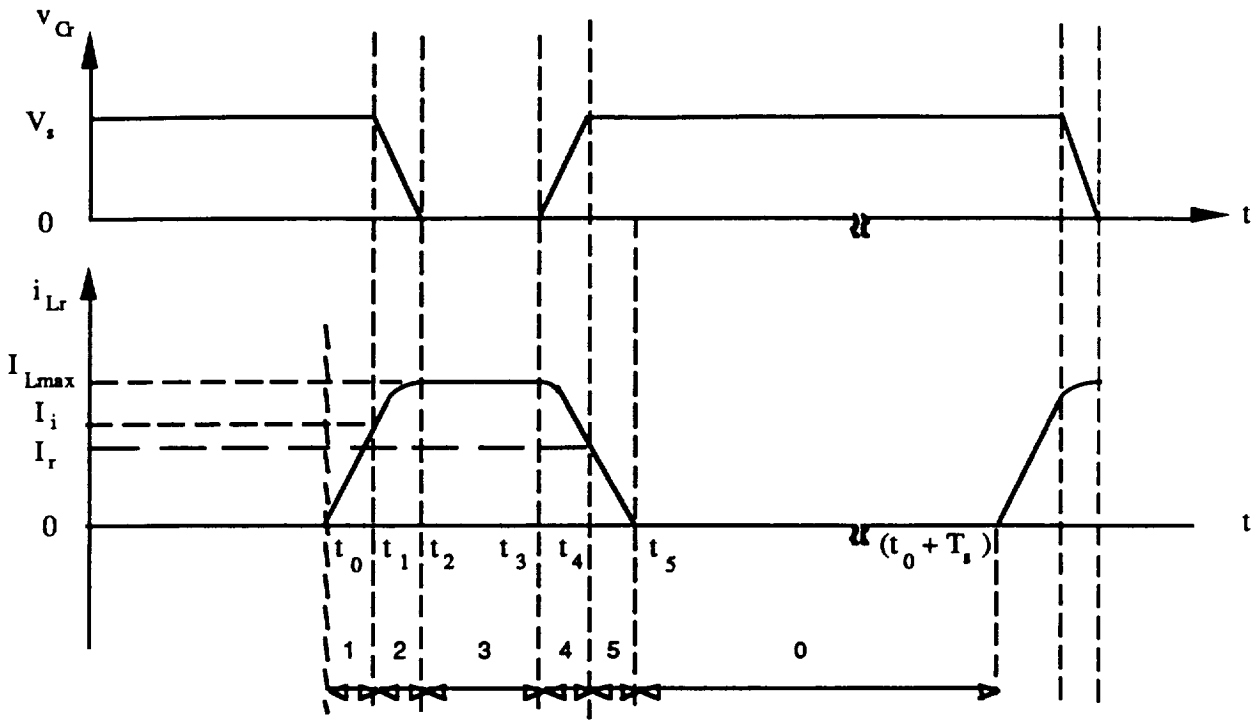

Figure 2.2. Operational Waveforms of the Parallel Resonant DC-Link.

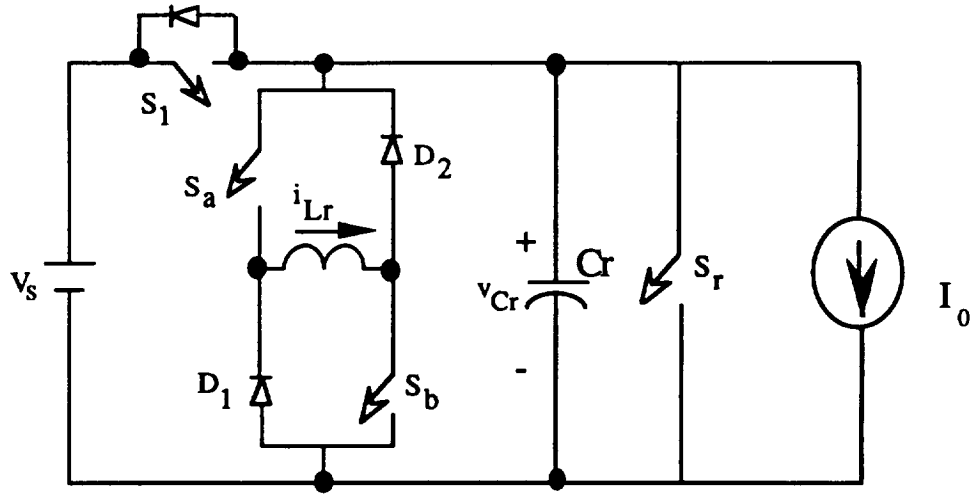

Figure 2.3. Parallel Resonant Link Circuit with Additional Switch Sr.

Mode 0 (Normal Operation) [5]

During this mode of operation, the circuit is operating as a stiff dc source with switch Sl conducting and switches Sa and Sb turned off (see Figure 2.4). Therefore, no current is allowed to flow in the resonant inductor and the LC circuit is at rest.

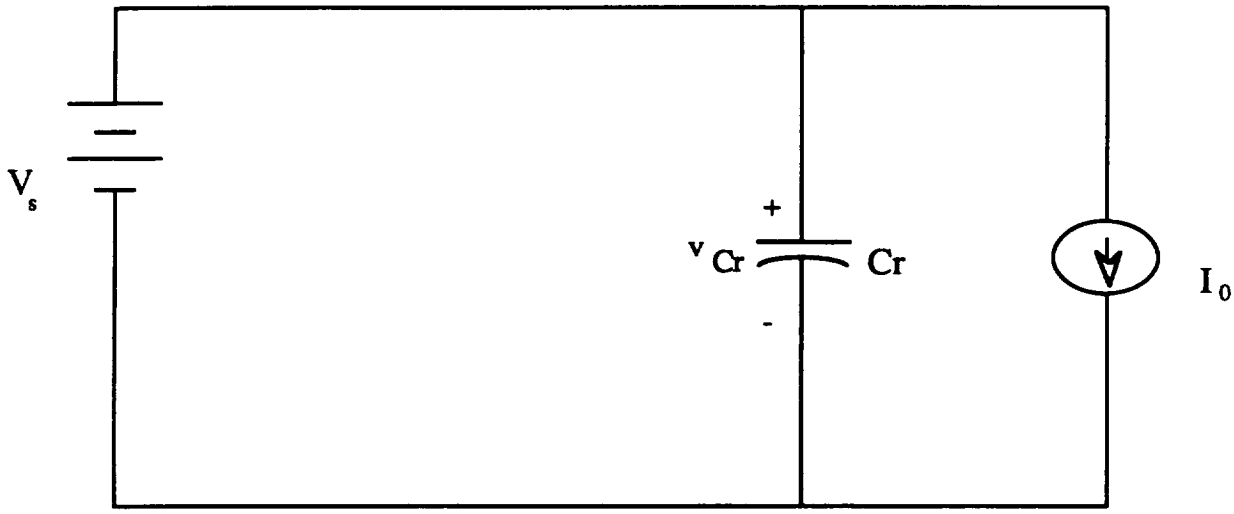

Figure 2.4. Equivalent Circuit for Mode 0.

Mode 1 [5]

When switching of the inverter is necessitated, switches Sa and Sb are simultaneously turned on, under zero current conditions to store energy in the resonant inductor (see Figure 2.5). The energy stored in the inductor ($E=.5\ Li^2$) must be sufficient in order to charge the resonant capacitor back to the value Vs after inverter switching has occurred. This critical level of stored energy is referenced by the inductor current I_{Lr} which increases linearly as follows:

$$I_L(t) = \frac{Vs}{Lr} t \tag{2.1}$$

The duration of this mode (T_1) is dependent upon the required energy needed in the inductor to charge the capacitor and ends upon the condition $I_{Lr}(T_1) = I_i$, where I_i represents the critical current level in the inductor.

$$T_1 = \frac{Lr \cdot I_i}{Vs} \tag{2.2}$$

The minimum value of I_i can be found by performing an energy balance on the capacitor and inductor as:

$$I_i = \sqrt{\frac{Vs^2 \cdot Cr}{Lr}} \tag{2.3}$$

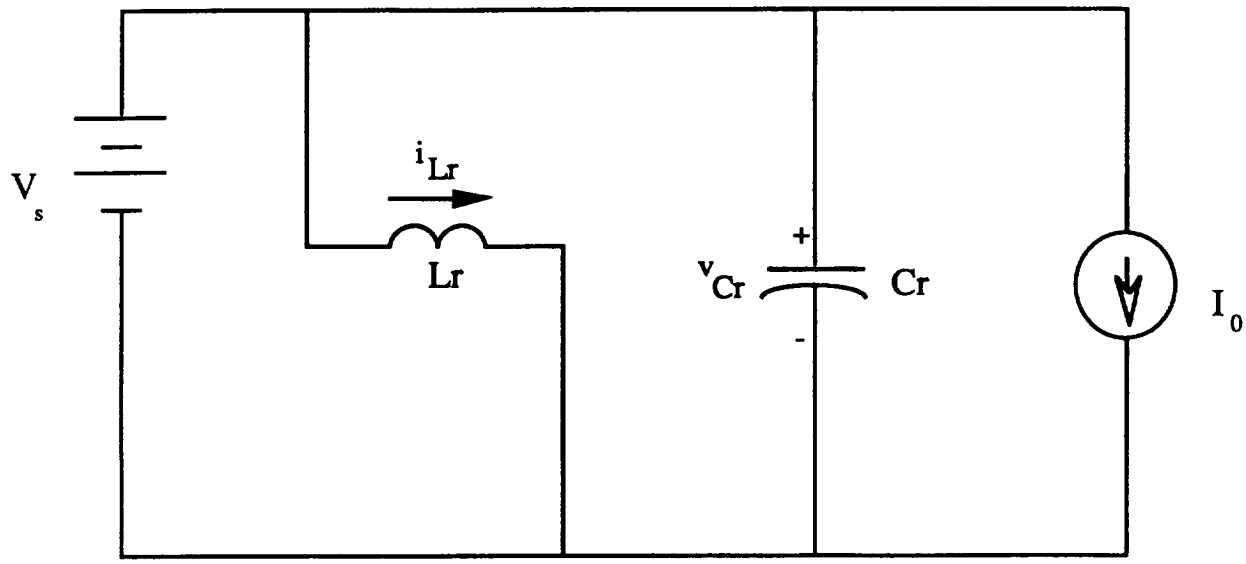

Figure 2.5. Equivalent Circuit for Mode 1.

Mode 2 [5]

Once the inductor current has reached I_i, switch S1 is opened under zero voltage conditions, disconnecting the circuit from the source Vs (see Figure 2.6). At this point, the LC circuit starts resonating with resonant frequency $\omega_r = 1/\sqrt{Lr \cdot Cr}$ and characteristic impedance, $Zr = \sqrt{Lr/Cr}$ as follows:

$$I_{Lr}(t) = \frac{Vs}{Zr}\sin(\omega_r t) + (Ii + Io)\cos(\omega_r t) - Io \tag{2.4}$$

$$V_{Cr}(t) = Vs \cdot \cos(\omega_r t) - Zr(Ii + Io)\sin(\omega_r t) \tag{2.5}$$

The capacitor voltage, V_{cr}, then decreases resonantly to zero. When $V_{cr} = 0$, this mode is completed with duration

$$T_2 = \frac{1}{\omega_r} \tan^{-1}\left(\frac{Vs/Zr}{Ii + Io}\right). \tag{2.6}$$

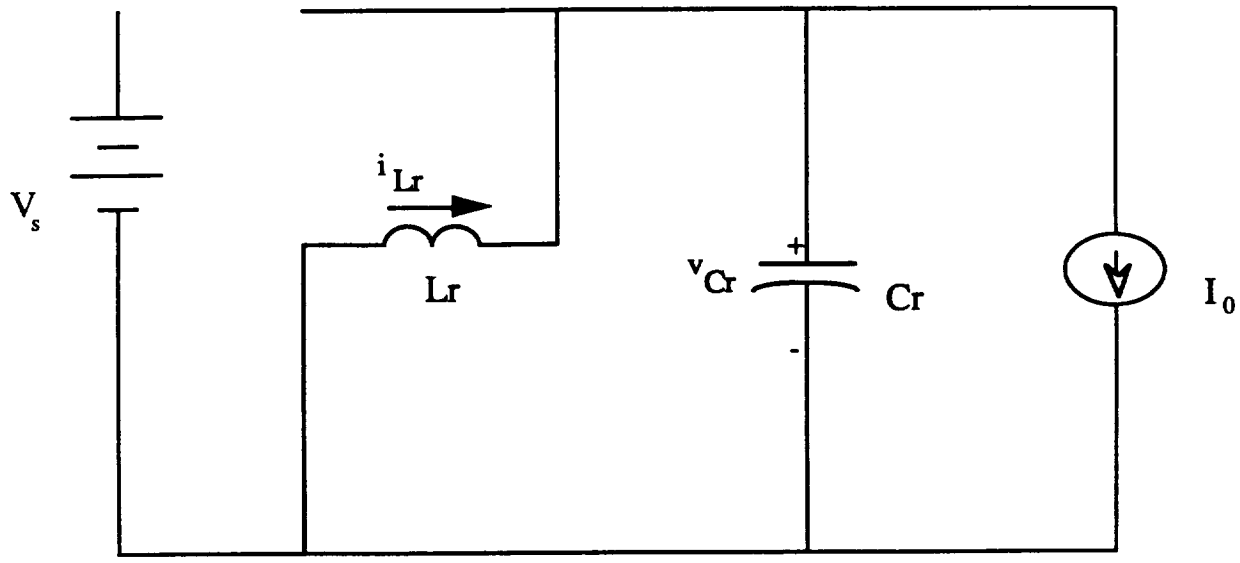

Figure 2.6. Equivalent Circuit for Mode 2.

Mode 3 [5]

During this mode of operation, the duration of the zero-voltage interval is set in order to allow the inverter switches to turn on/off. The resonant capacitor voltage is clamped at zero by switch Sr while the inductor current circulates in two parallel paths created by diodes D1 and D2 (see Figure 2.7) so that

$$V_{cr} = 0 \tag{2.7}$$

$$I_{Lr} = I_{L\max} = \sqrt{(Ii+Io)^2 + \left(\frac{Vs}{Zr}\right)^2} - Io \tag{2.8}$$

It is during this mode that the inverter switches change states under zero voltage conditions while the load current Io circulates through the inverter, switch Sr, and diodes D1 and D2.

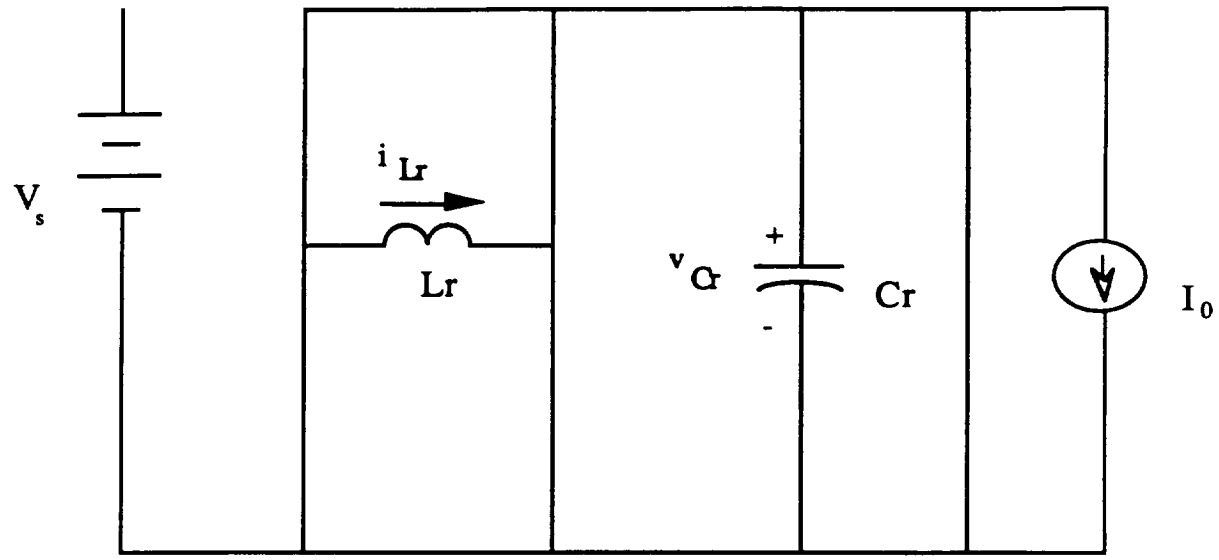

Figure 2.7. Equivalent Circuit for Mode 3.

Mode 4 [5]

The end of the zero-voltage interval marks the beginning of Mode 4. At this time switches Sa and Sb are opened under zero-voltage conditions to charge the capacitor voltage V_{Cr} to the supply voltageVs (see Figure 2.8). Energy previously stored in the inductor during Mode 1 flows through diodes D1 and D2 to charge the capacitor voltage as follows:

$$I_{Lr} = (I_{L\max} - Io)\cos(\omega_r t) + Io \tag{2.9}$$

$$V_{Cr} = Zr(I_{L\max} - Io)\sin(\omega_r t) \tag{2.10}$$

The duration of the interval can be found from the condition V_{Cr}=Vs as

$$T_4 = \frac{1}{\omega_r}\sin^{-1}\left(\frac{Vs/Zr}{I_{L\max} - Io}\right). \tag{2.11}$$

The energy remaining in the inductor at the end of this mode is characterized by the current:

$$I_{Lr}(T_4) = Ir = \sqrt{(I_{L\max} - Io)^2 - \left(\frac{Vs}{Zr}\right)^2} + Io \tag{2.12}$$

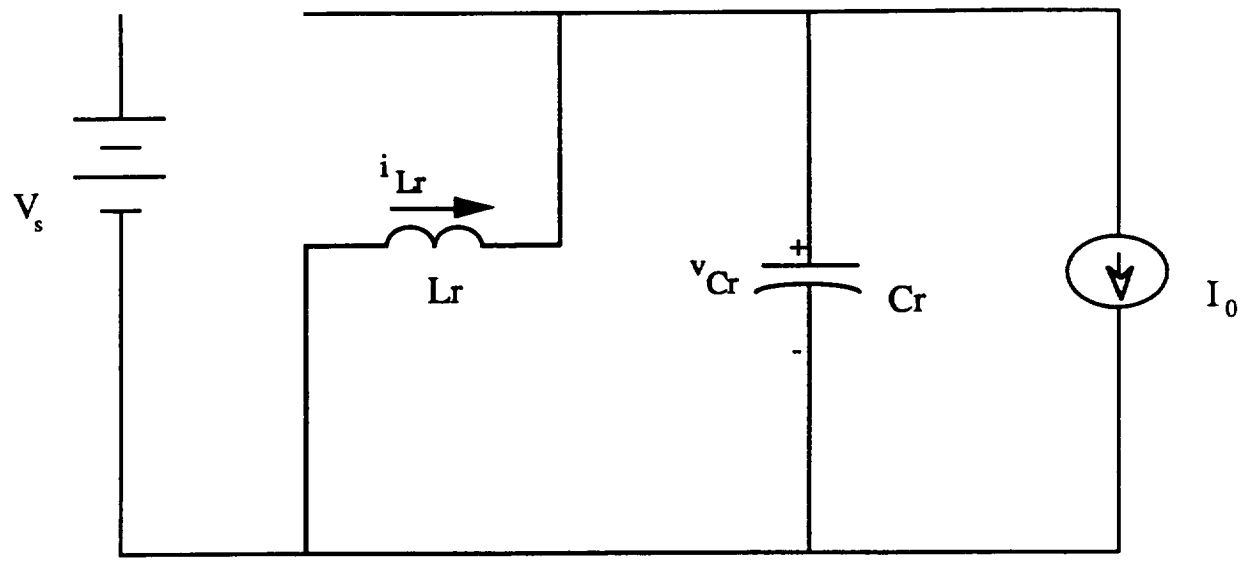

Figure 2.8. Equivalent Circuit for Mode 4.

Mode 5 [5]

Once the capacitor voltage V_{Cr} is increased slightly above the source voltage Vs , the diode in antiparallel with switch Sl begins to conduct and any additional energy stored in the resonant inductor is returned to the source through this path (see Figure 2.9). As the diode begins to conduct, switch Sl is turned on under zero-voltage conditions. The inductor current linearly decreases to zero at which point diodes D1 and D2 are turned off and one switching cycle of the circuit is complete. Thus for this mode

$$V_{Cr} = Vs \qquad \text{and} \tag{2.13}$$

$$I_{Lr}(t) = -\frac{Vs}{Lr}t + Ir. \tag{2.14}$$

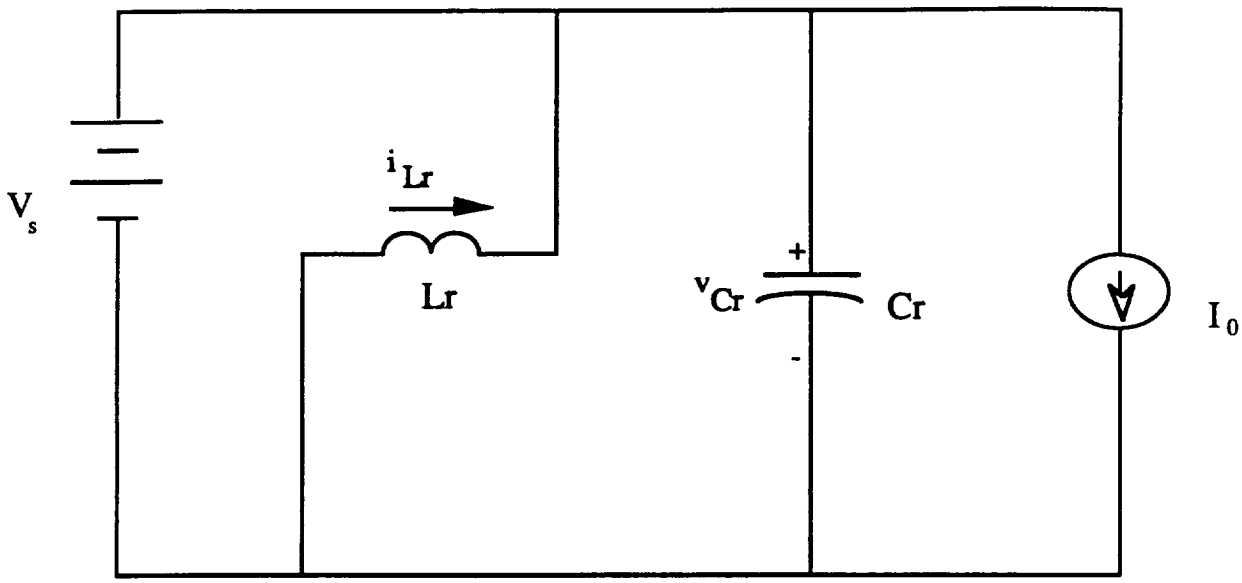

Figure 2.9. Equivalent Circuit for Mode 5.

Chapter 3

EXPERIMENTAL SETUP

In the previous chapter, the operation of the parallel resonant link was discussed and described by equivalent circuits for each mode of operation. This chapter will present the implementation of the circuit as well as the selection of the circuit components. The control algorithm will also be presented in this chapter.

Inductor and Capacitor Design

Capacitor Cr must have a voltage rating of at least 270 V and be capable of carrying very large currents during Mode 4 of the resonant link's operation. A General Electric 97F8585 DC capacitor was selected which has a value of 0.5μF and a voltage rating of 1000 V. This capacitor was chosen because it is designed to carry large pulse currents.

The inductor design was somewhat more critical because of the high peak currents that it must conduct (see Figure 2.2). A 5μH inductor was designed which was capable of carrying approximately 200 amperes of current without saturating. The inductor was constructed using two Magnetics, Inc. powdered iron cores (Part No. 58868-A2) which were epoxied together and wrapped with nine turns of no. 7 copper-braided cable. This

combination resulted in a resonant frequency, f_r of 100 kHz and a characteristic impedance of 3.16 ohms.

Semiconductor Devices

Switches Sl, Sa, Sb, and Sr (see Figure 2.3) are all implemented using Insulated Gate Bipolar Transistors (IGBTs). The switches must have a voltage rating of at least 270 V. The largest current which must be conducted by switch Sl is approximately 220 A, which is the sum of the maximum inverter current (Io=100 A) and the peak inductor current ($I_{L\,max}$≈120A). The frequency of the peak current will depend largely upon how often the inverter switches are required to switch by both the Hall Effect sensors and the speed/position controls. Inverter operation in six step mode will result in the lowest frequency and smallest average value of current through switch Sl. The RMS value of the current is also the lowest for this case as opposed to other regulation schemes such as pulse width modulation (PWM), which will be discussed in greater detail later in this chapter. With a margin of safety in mind, an IGBT with a current rating of 300A was selected for this switch.

The remaining switches Sa, Sb, and Sr are not subject to current levels quite as high as those seen by switch Sl. Switches Sa and Sb are required to carry the resonant inductor current (I_{Lr}) which must be maintained at $I_{L\,max}$ during the zero voltage interval (Mode 3). Therefore, the current rating for these switches need only be 100A due to the small duty cycle / average value of inductor current. Switch Sr is added to the original waveshaping circuit (see Figure 2.1) in order to clamp the bus at zero volts during the

zero-voltage interval. This switch would likely not be necessary if the physical dimensions of the connections between the waveshaping circuit and inverter could be minimized. From laboratory experience it was found that these long leads introduced a significant inductance into the circuit. Hence the need for switch Sr to limit the ringing of the bus voltage during the zero voltage interval. Switch Sr must have a voltage rating of at least 270 V, but it must be capable of carrying minimal current. This is due to the parallel paths through which the load current circulates. These paths are created by the diodes in antiparallel with switches T1-T6 along with the path created by diodes D1 and D2. Therefore as a worst case scenario, the largest current seen by switch Sr would be the peak inverter current, Io. Powerex IGBT's were selected for implementation in the link circuit. All four switches were implemented using 600 V devices rated at 400 A.

Similar to switches Sa and Sb, diodes D1 and D2 must be capable of conducting the peak inductor current (I_{Lmax}) during Mode 4 of the resonant link's operation. For this function, Powerex C-series 600 V diodes (Part No. CS240610) rated at 100 A were chosen.

Block Diagram of the Parallel Resonant DC Link circuit

Figure 3.1 is a block diagram for the PRDCL circuit as it has been implemented. The PRDCL operation is initiated by the trigger signal sent from the controller board which sets the flip-flop that controls switches Sa and Sb. Current is then linearly built up in the resonant inductor until the critical level, Ii, where it is monitored by an American Aerospace Controls 200 A bidirectional current sensor (Part No. S273). This current

sensor features a full scale output of 5 V with no dc offset. When the inductor current reaches Ii, the output of the current sensor triggers a voltage detector (labeled Ii voltage detector in Figure 3.1) which sets the flip-flop controlling switch Sl. Mode 2 now begins as the bus voltage falls to zero. Note that the bus voltage is measured and fed back into a zero-voltage detector. The output of this detector is used to trigger a 555 timer which is operated in a monostable mode to set the duration of the zero voltage interval. The zero-voltage interval signal is then used to perform two critical functions. First, the signal is used to gate switch Sr and clamp the bus voltage at zero volts for a predetermined time. Second, it is fed into the flip-flop that controls switches Sa and Sb. Here the falling edge of the signal resets the flip-flop so the switches are turned off under zero-voltage conditions. This marks the end of the zero voltage interval as the bus voltage is now increased resonantly until it reaches Vs. Similar to the operation of the zero-voltage detector, another voltage detector, designated the Vs voltage detector, is used to sense the bus voltage returning to Vs. The output of this detector is used to reset the flip flop which controls switch Sl.

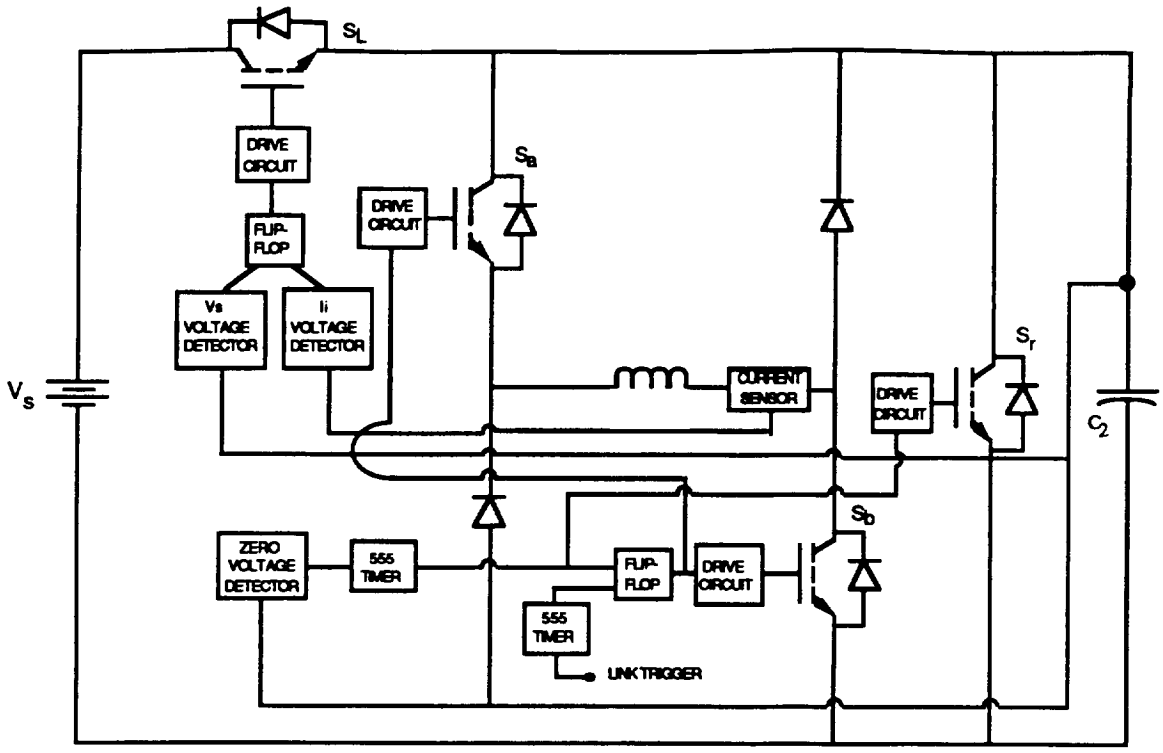

Figure 3.1 Block Diagram of the PRDCL Circuit.

System Block Diagram

A system block diagram is shown in Figure 3.2. In this diagram the link circuit is combined with the three phase inverter. Note that the link trigger is provided by the differentiation of the inverter drive signals combined with the current controller output (hereafter referred to as the PWM signal). Differentiators are used to provide the falling edge signal necessary to trigger the 555 timer of the link circuit (see Figure 3.1). The drive signals are decoded from the output of Hall Effect sensors by a 20 pin DIP Generic Array Logic (GAL) integrated circuit. The GAL features electrically erasable cell technology that allows for easy reprogramming. This method of decoding the Hall sensors allows a great deal of flexibility as the GAL can be programmed to decode any sequence of sensor outputs specific to a particular motor. The particular GAL chosen, a GAL16V8B

manufactured by Lattice, contains a programmable 64X32 AND array, utilizing up to sixteen inputs and eight outputs. The direction signal along with the three Hall effect signals are implemented as inputs to the GAL. Six outputs of the GAL correspond to the drive signals for the IGBT's which make up the inverter. This GAL is characterized by its low input power specifications as well as a small propagation delay time of 10 ns.

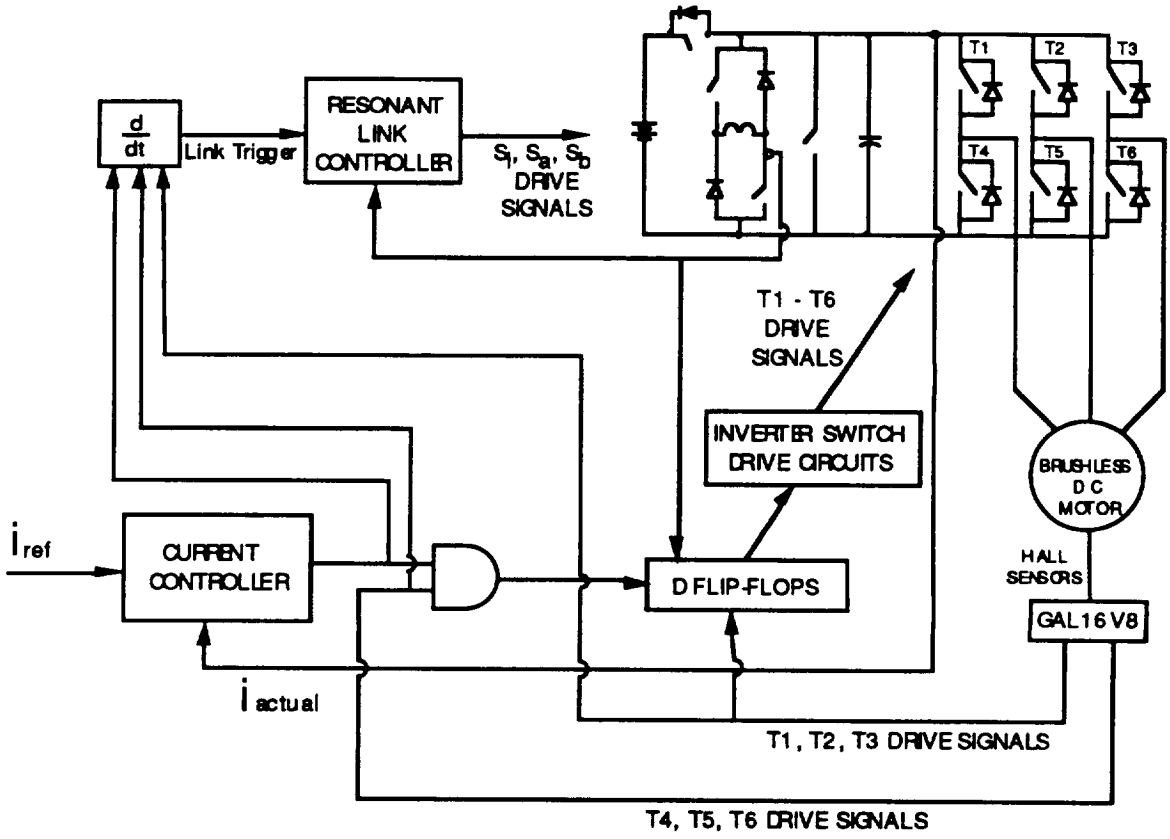

Figure 3.2 System Block Diagram.

The inverter drive signals are determined from the outputs of the GAL. The GAL ensures that only two switches are conducting at a time, one top switch and one bottom switch in such a way that the bus is never shorted (i.e., switches T1 and T4 are not allowed to conduct at the same time). Additionally, to achieve ZVS, the zero-voltage interval is sensed by the clock signals of D flip-flops which control the inverter switches' drive circuits. This prevents the inverter switches from changing states except during the zero-voltage interval.

When the three phase inverter is operating in the six step mode (no regulation), the PWM signal is a logical 1 and no additional triggers are sent to the link circuit. Regulation of the current flowing in the brushless dc motor is implemented as in Figure 3.3. Ideally, the individual phase currents of the motor would be monitored using current sensors. Due to constraints in board space for the controller built for MSFC, an alternative approach was taken. As an approximation to the actual motor phase currents, the input current to the inverter is sensed using a current sensor. Note this current is the motor current as long as one top switch and one bottom switch of the inverter are closed. This current is compared to a reference current determined from position and speed measurements. In the event the current command (represented as Iref) is for zero current, as would be necessitated for position control (speed of zero), the bottom switches of the inverter are opened, preventing current flow in the motor. In a regulatory role, as would be typical for speed control as well as position control, the average power sent to the motor is controlled by the resonant link circuit as in Figure 3.3.

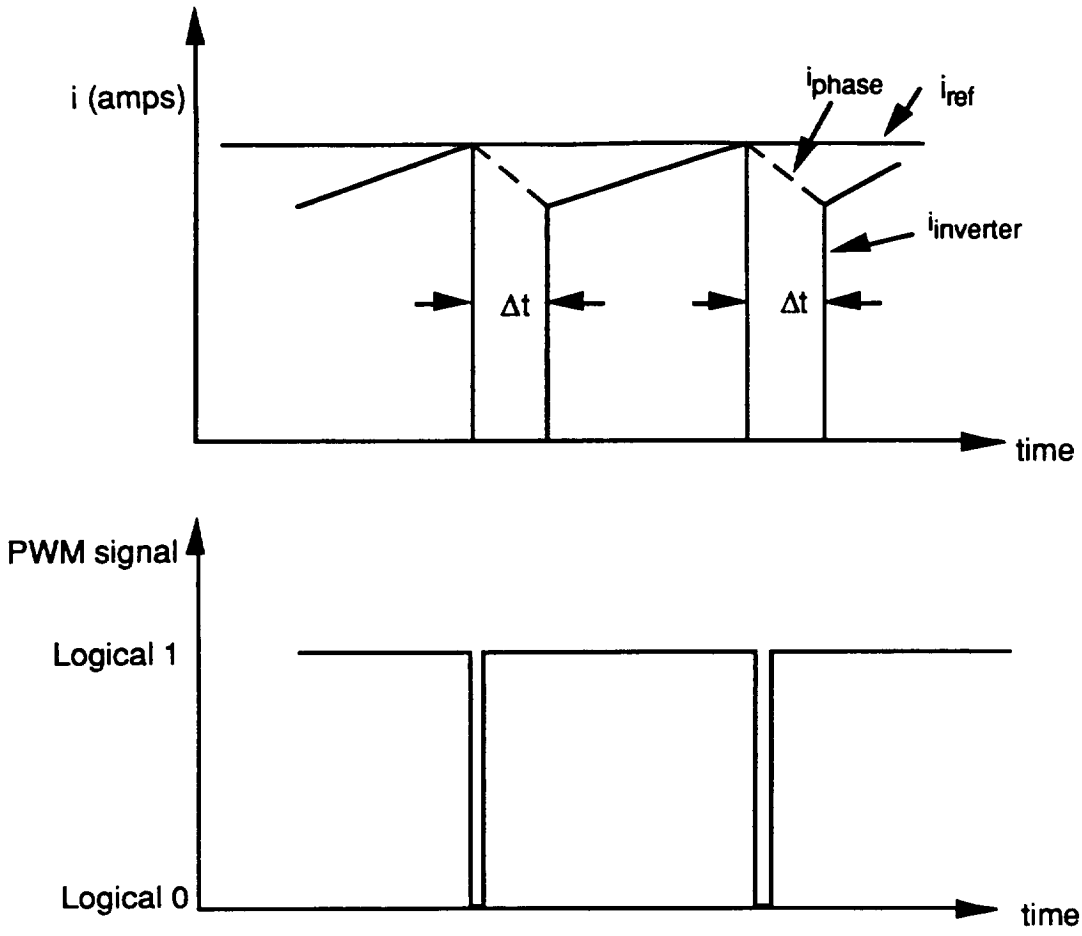

Figure 3.3 Current Control Algorithm and Corresponding PWM Signal.

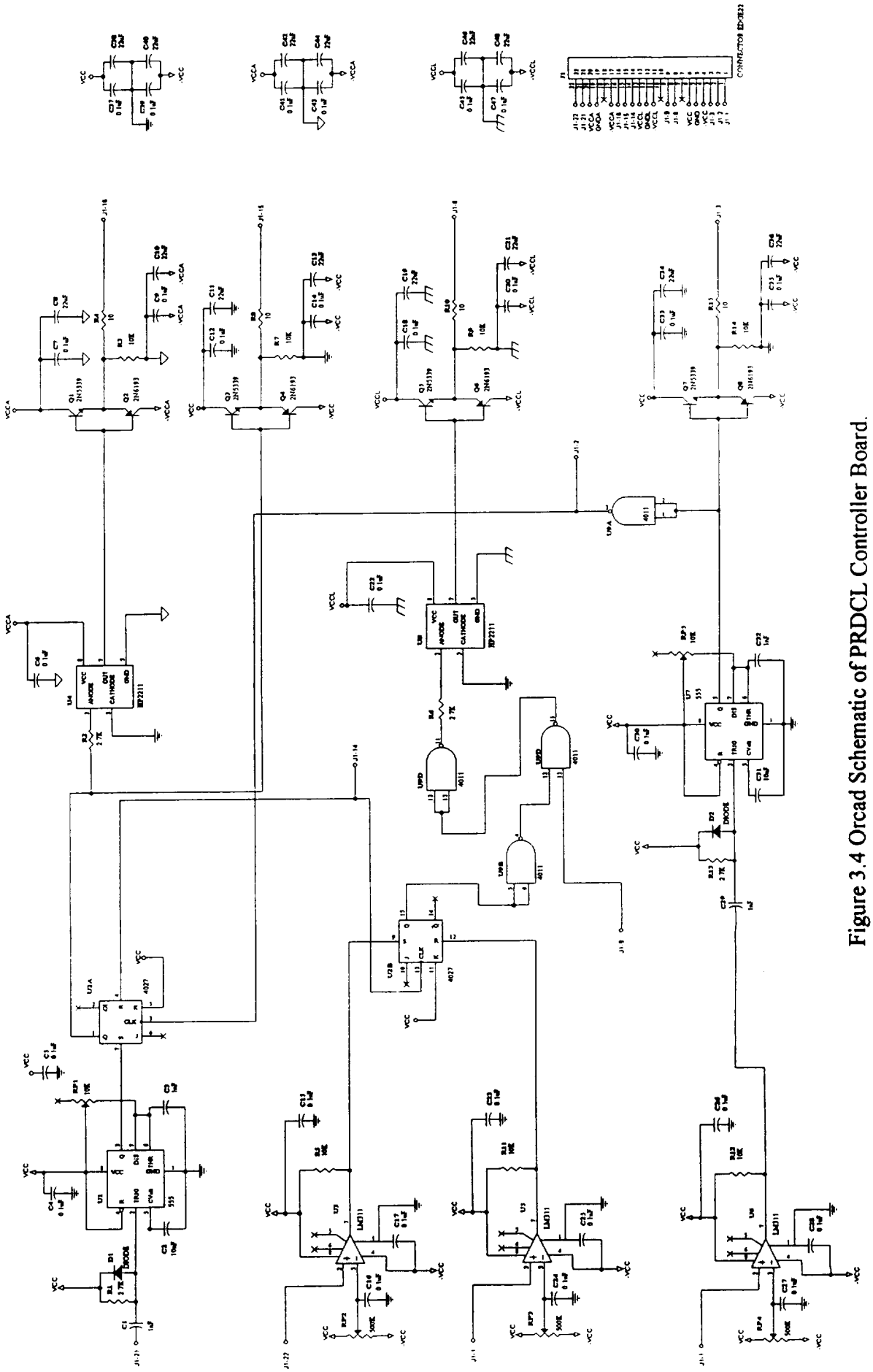

Figure 3.4 Orcad Schematic of PRDCL Controller Board.

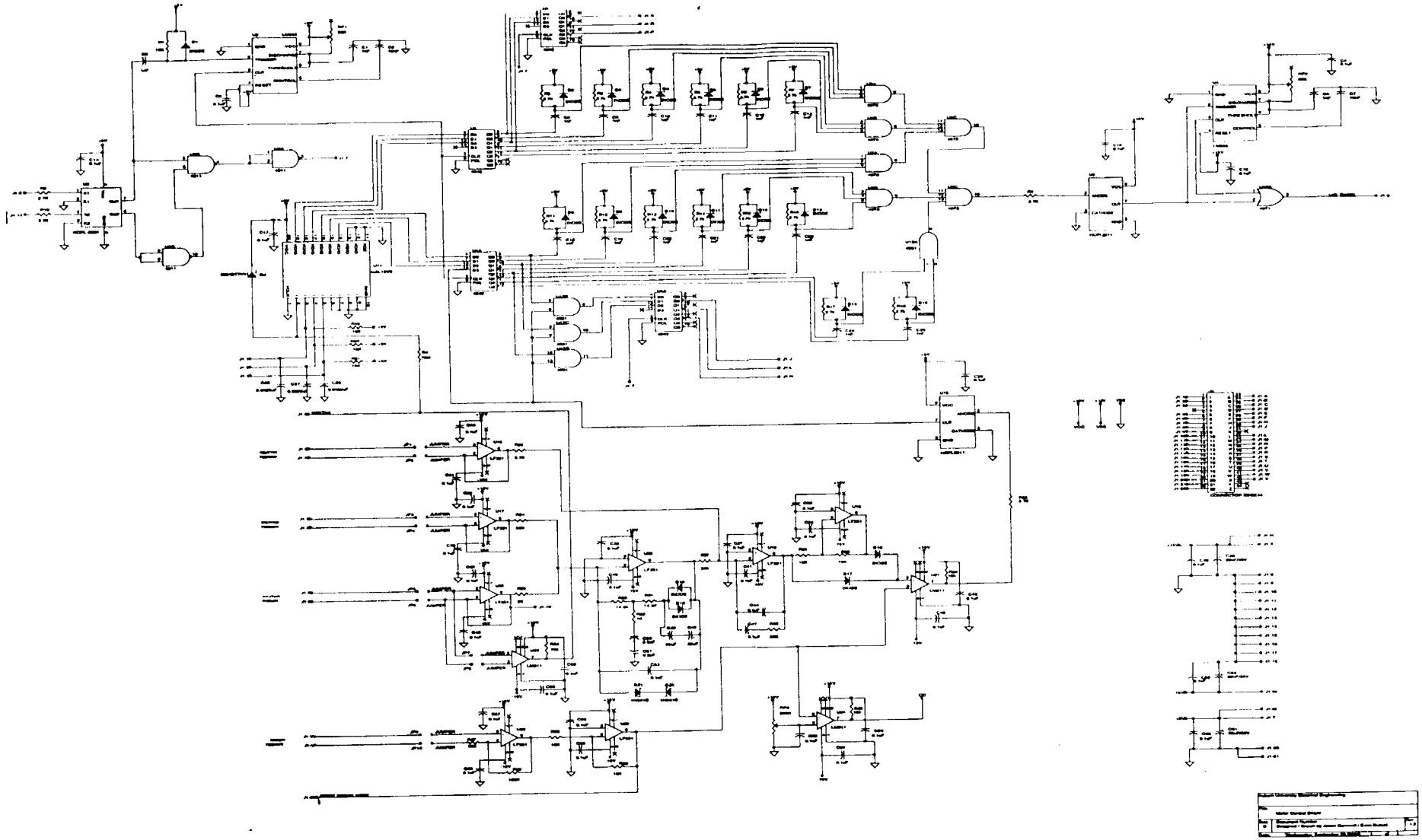

Figure 3.5 OrCAD Schematic of Inverter Controller Board.

Chapter 4

EXPERIMENTAL RESULTS

This chapter will discuss experimental results obtained using the setup described in the previous chapter. Two experimental setups have been constructed at Auburn University. One of these will be referred to as the AU controller. It was tested in the laboratory at Auburn University and uses different component values from those described earlier in this report. The second controller, referred to as the MSFC controller, was constructed using earlier calculated component values. It was tested in the EB24 laboratory at Marshall Space Flight Center during the week of December 14-17, 1995.

AU Controller

This controller was used to drive both a Reliance Electric brushless dc motor as well as an Inland Motor like those used for testing at MSFC. The ratings of the Reliance motor are as follows:

Rated power - 5 Hp

Rated speed - 4000 RPM

Rated current - 30 A

Rated voltage - 270 V

Commutation signals are provided by Hall effect sensors. The Reliance motor is loaded by a 4.5 kW DC generator connected in a separately-excited configuration. The field circuit for the generator was supplied by a variable DC supply. A variable resistance was connected to the generator armature terminals. The output power of the DC generator can be varied via the variable field supply or by changing the resistance.

The input voltage for the AU controller was provided by rectifying the output of a variable AC supply. The range of input voltages was 0 - 100 V. All semiconductor

switches of the PRDCL circuit and three-phase inverter are International Rectifier IRFP250 power HEXFET MOSFETs with ratings of 200 V and 33 A. Power MOSFETs were implemented as opposed to IGBT's due to their availability during a world wide shortage of all power semiconductors at the time of purchase. All diodes are Motorola 1N3913. The inductor and capacitor values are those described in Chapter 3.

MSFC Controller

The implementation of this controller is exactly as depicted in Chapter 3. In addition, two circuit boards were designed and fabricated to interface with the test setup in the EB24 laboratory at MSFC. One of the circuit boards controlled the PRDCL while the other circuit board contained the GAL used to decode the Hall signals as well as the other controls for the three phase inverter. In addition, a three phase inverter on loan from the EB24 laboratory was rewired / modified in order to effectively interface with the PRDCL.

Figure 4.1 is a plot of V_{Cr}, which is the voltage at the input to the inverter, and the resonant inductor current, I_{lr}, for an input voltage of approximately 70 V, a zero voltage interval of 10 μs and a load current Io of approximately 3 A. These waveforms closely resemble those of Figure 2.3 while the conduction losses of the PRDCL can readily be seen by the slight negative slope of the inductor current during the zero voltage interval. The peak value of the inductor current taken from the scope trace is approximately 34 A compared to a theoretical value of :

$$Ii = \sqrt{\frac{70V^2 \cdot .5\mu F}{5\mu C}} = 22.1A, \text{ and } \quad I_{L_{max}} = \sqrt{(22.1A + 3.0A)^2 + (\frac{(70V)^2}{3.16\Omega})} - 3.0A = 30.5A$$

using equations 2.3 and 2.8. The difference in these values reflect the assumptions made in Chapter 2 of the ideal / lossless nature of all circuit components.

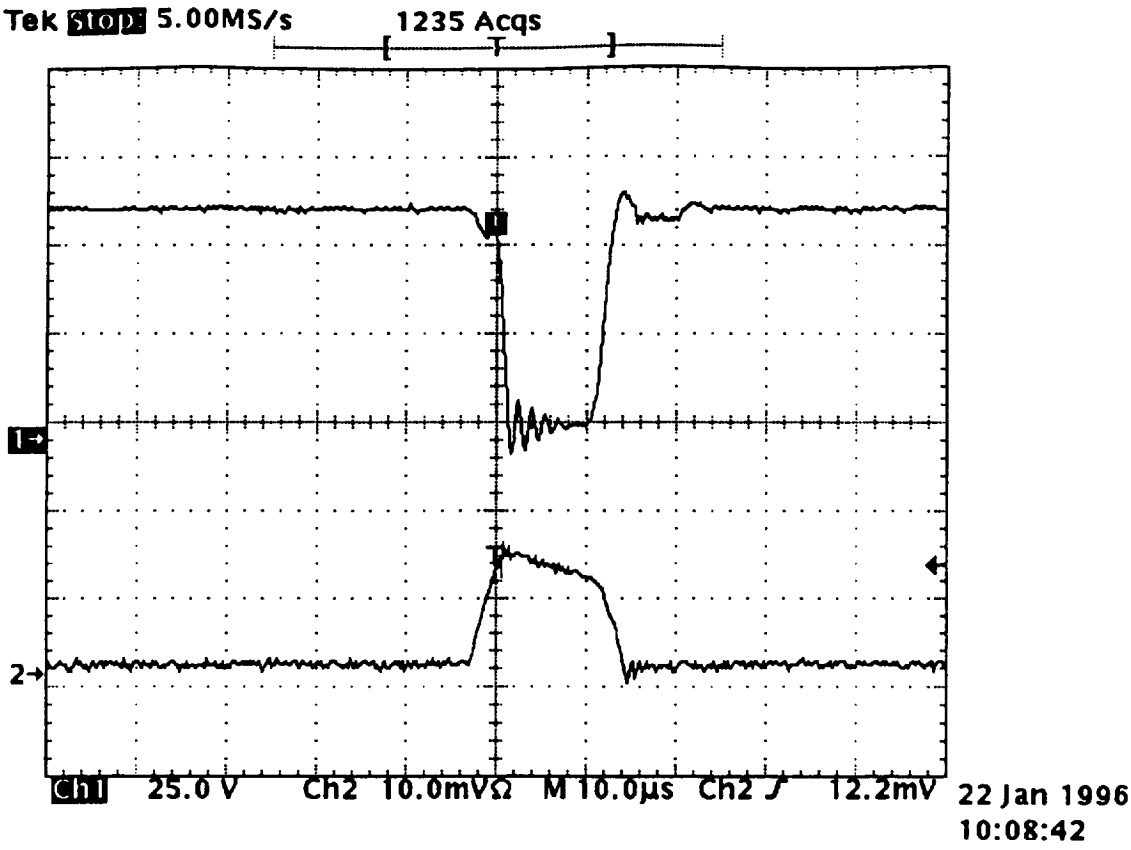

Figure 4.1. Voltage V_{Cr} and Inductor Current I_{lr} (bottom) vs. Time for 70 V Input.

The ZVS of the inverter switches is illustrated in Figure 4.2 which depicts the input voltage to the inverter along with the drive signals for each of the top switches of the inverter during a switching transition of the inverter. Note that for a drive signal output of 5 V, logical 1, the IGBT is conducting. At this particular transition, the first switch is turned off while the second switch is turned on and the status of the third switch remains unchanged. It can be seen from this that the switches are only allowed to change states only during a zero voltage interval.

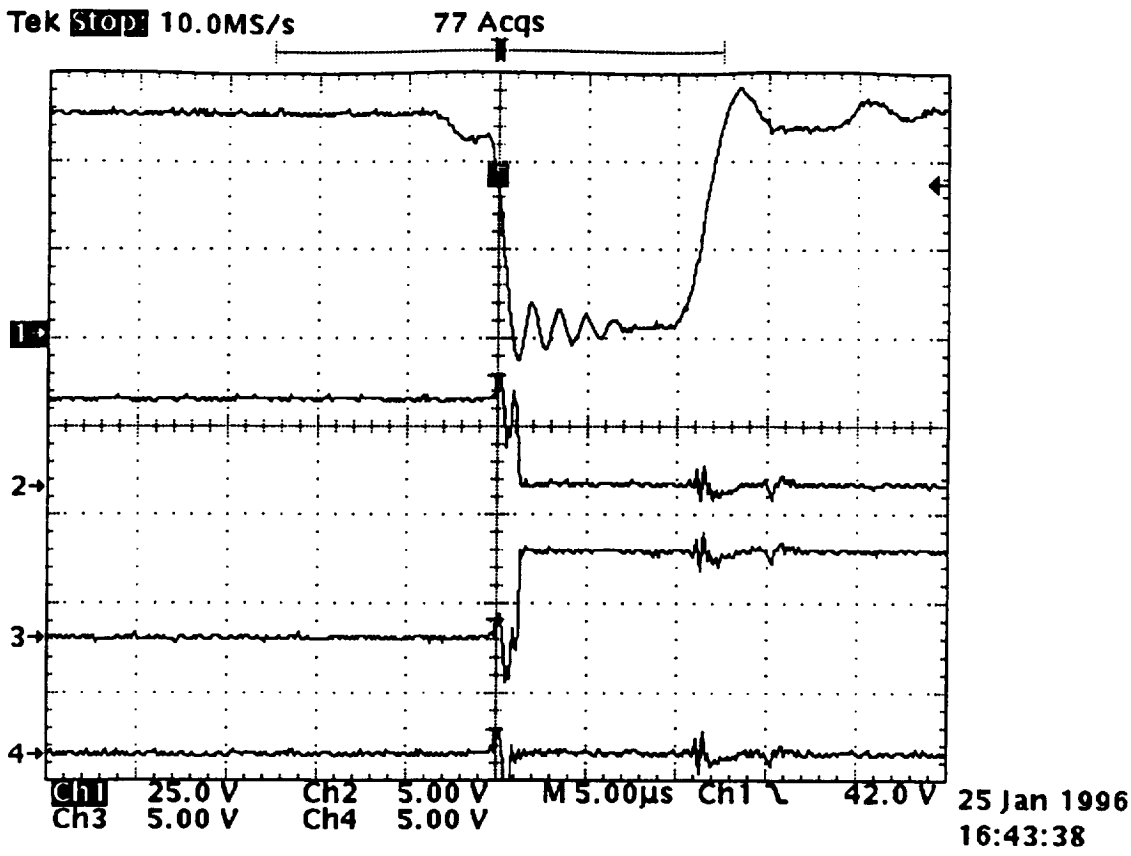

Figure 4.1. Voltage V_{Cr} and IGBT Drive Signals vs. Time

The current control algorithm discussed in the previous chapter is illustrated by the following scope traces. Figure 4.3 depicts waveforms of the Phase A current with an input voltage of 70 V. The top current waveform is of the motor operating in the six-step mode - no current regulation. Similarly, the bottom waveform shows the same phase current limited to 2 A. The PWM signal generated during this regulation is shown in Figure 4.4. Note that each time the PWM signals falls to zero volts, the link circuit receives a trigger signal and the inverter current falls to zero during the zero voltage interval while the phase current decreases linearly due to the back emf of the motor (as shown in Figure 3.3).

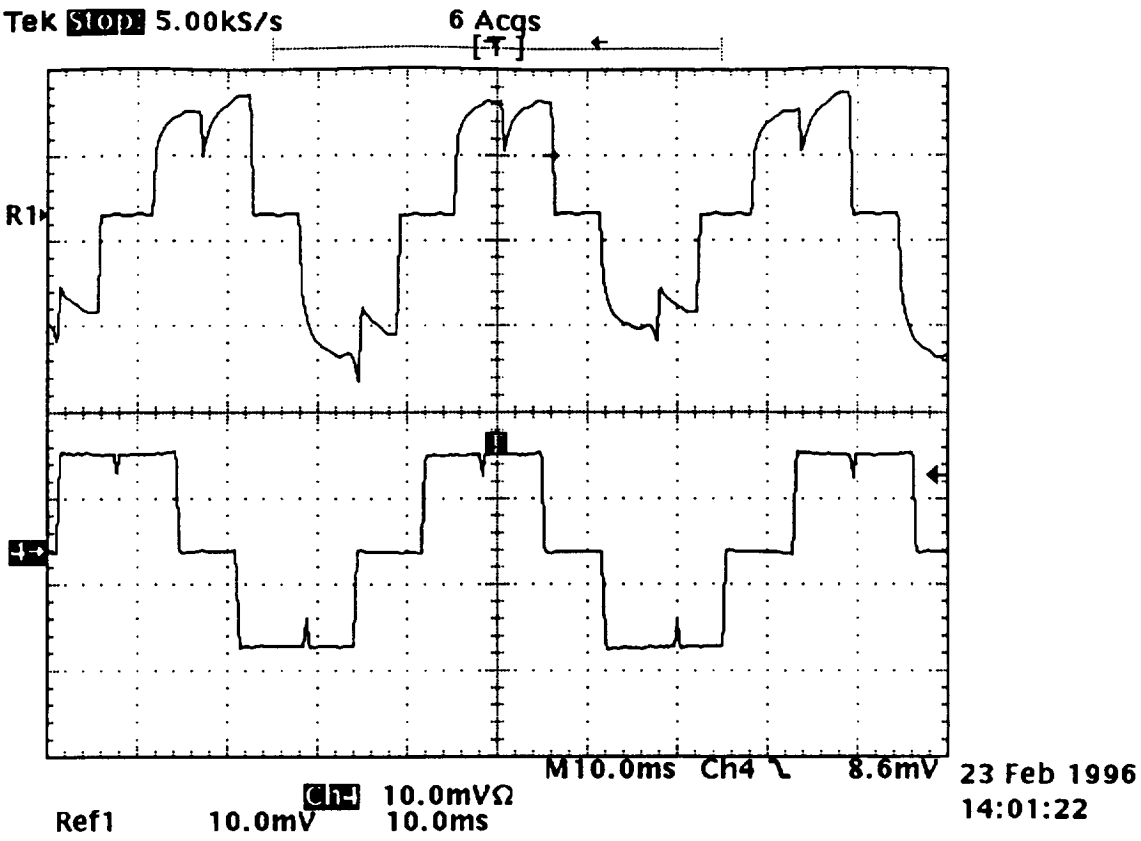

Figure 4.3. Phase A Currents: Top-No Regulation, Bottom-Regulated to 2 A.

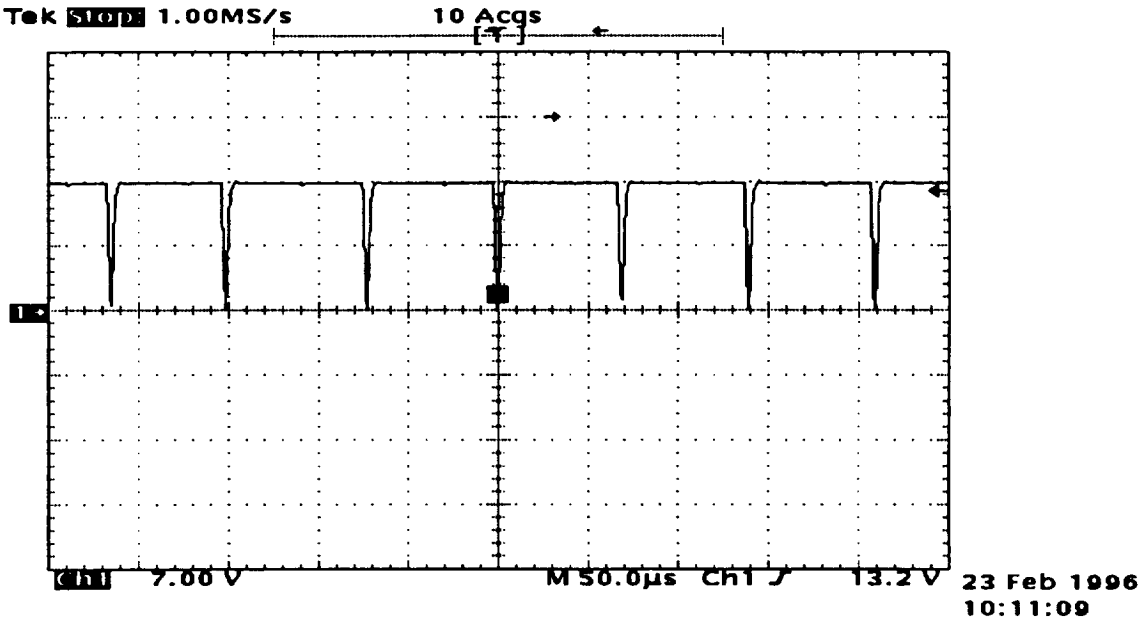

Figure 4.4. PWM Signal vs. Time During Regulation.

Chapter 5

CONCLUSION

This project was focused upon the design of a zero-voltage switching inverter to be used in conjunction with a brushless dc motor in an electromechanical actuation (EMA) system. This EMA sytem is being considered for implementation in future space transportation applications. Position control of the actuator is achieved by controlling the flow of energy to the motor. The ZVS characteristics of the inverter would greatly improve the present approach taken at MSFC due to reductions in EMI and switching stresses/losses.

In order to achieve ZVS of the inverter switches, a waveshaping circuit must be added to the front end of the inverter in order to condition the voltage input to the inverter. This waveshaping circuit causes the input voltage to ring to zero for a short period of time, during which the semiconductors that make up the inverter are turned on/off. There are many resonant circuits that would perform this task but the particular circuit chosen a Parallel Resonant DC Link (PRDCL), was found to be advantageous over other similar choices. Most importantly, the circuit utilizes a single resonant inductor and capacitor as well as only four semiconductor switches. However, the number of semiconductor switches could be further reduced if the circuit were packaged in such a manner that the physical connections between the PRDCL and the inverter could be minimized. The operation of the PRDCL was described in Chapter 2, where the six modes of the circuit's operation were analyzed using equivalent circuits assuming ideal circuit components. The implementation of the link circuit as well as the overall system was treated in Chapter 3. The current control scheme that was employed was also described and schematics of the boards were also included. Experimental results along with scope traces were given in Chapter 5.

Two implementations of the ZVS inverter were built and used successfully to control the brushless DC motors discussed in the previous chapter. However, the starting of the 12 pole Inland motor was not as reliable as the starting of the 5 HP Reliance motor in the lab at Auburn. The main objective of this project was to improve upon the previous work done for the MSFC Propulsion Division by Auburn University. First, a substitute for the LM621 integrated circuit responsible for decoding the Hall effect signals was identified in the GAL. This approach allows for a great deal of flexibility as the GAL can be programmed to decode any sequence of Hall signals specific to a particular motor. Secondly, the previously designed controller required a great deal of tuning/adjusting of potentiometers in order to achieve proper link circuit operation. This problem is corrected by the PRDCL as the only critical potentiometer setting is used to set the inductor current trip level, Ii. Lastly, improving upon the use of a single current sensor to approximate the motor current in the control scheme was researched. This problem was not addressed as the additional circuitry required to monitor the individual phase currents could not be placed on the printed circuit boards because of limitations on the phsical size of the controller . However, this problem could likely be dealt with only slight modification of the current design.. The GAL is currently not being fully utilized. The GAL's capabilities could be furthered by utilizing additional inputs to implement the operation of the D flip-flops on the controller board. The removal of these IC's along with the associated traces would likely free up additional board space that could be used to implement a control scheme where the individual phase currents would be monitored.

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